

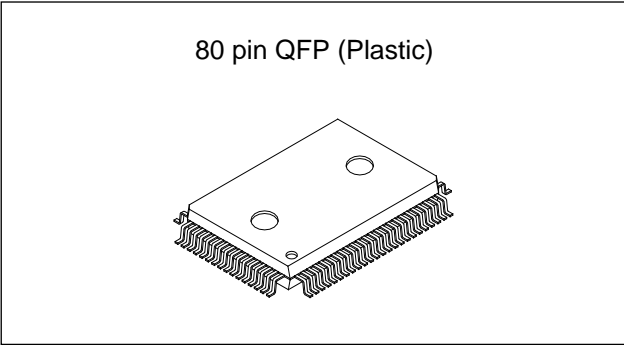
CXP84632/84640/84648

CMOS 8-bit Single Chip Microcomputer

Description

The CXP84632/84640/84648 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, I²C bus interface, remote control reception circuit, PWM output, and 32kHz timer/counter besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP84632/84640/84648 also provides a sleep/stop function that enables lower power consumption.



Structure

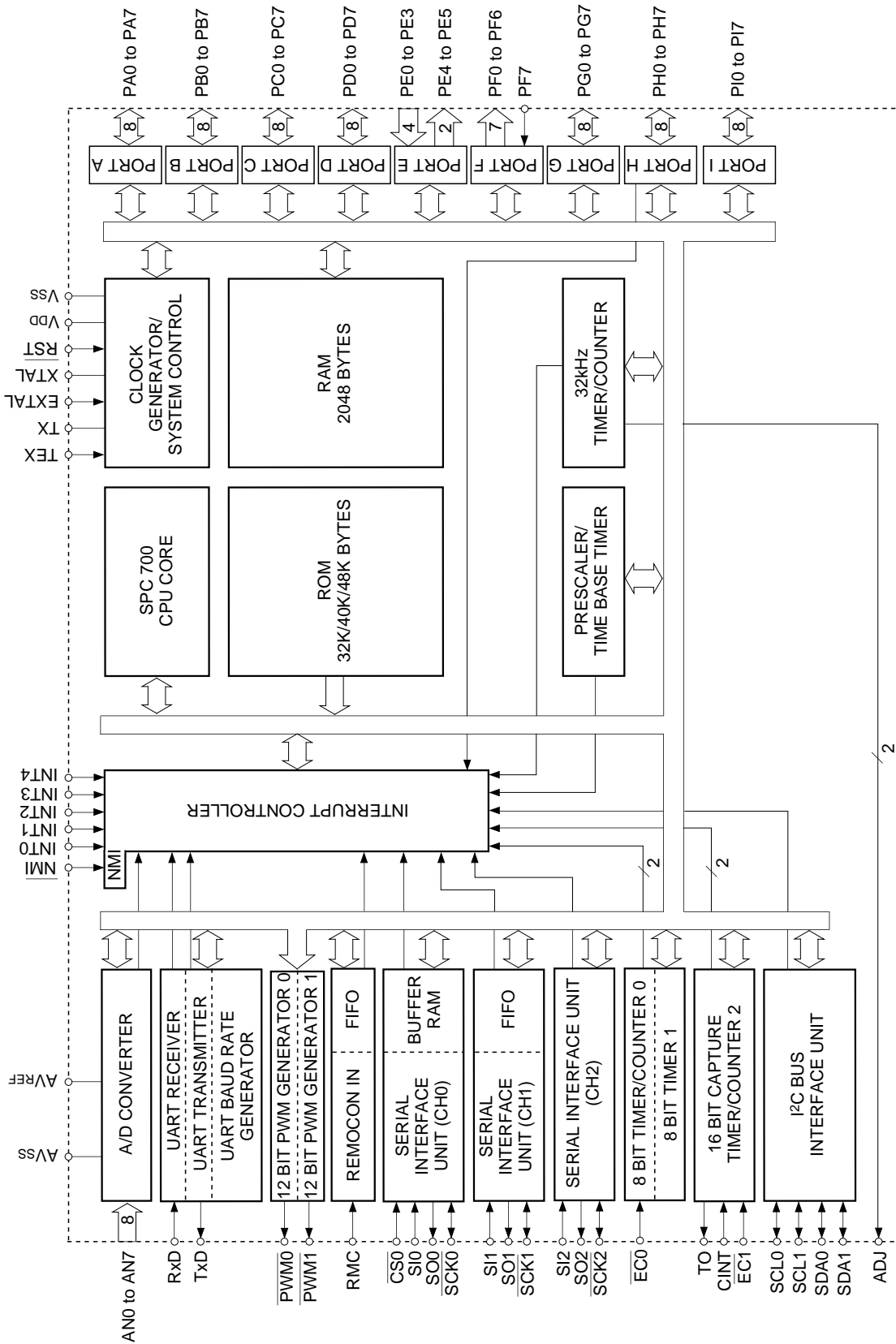
Silicon gate CMOS IC

Features

- Wide range instruction system (213 instructions) to cover various of data.
 - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
 - 250ns at 16MHz operation (4.5 to 5.5V)
 - 333ns at 12MHz operation (3.0 to 5.5V)
 - 122µs at 32kHz operation (2.7 to 5.5V)
- Incorporated ROM capacity
 - 32K bytes (CXP84632)
 - 40K bytes (CXP84640)
 - 48K bytes (CXP84648)
- Incorporated RAM capacity
 - 2048 bytes
- Peripheral functions
 - A/D converter
 - 8 bits, 8 channels, successive approximation method (Conversion time 20µs/16MHz)
 - Serial interface
 - Start-stop synchronization (UART), 1 channel
 - Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 1 channel
 - Incorporated 8-bit, 10-stage FIFO (Auto transfer for 1 to 10 bytes), 1 channel
 - 8-bit clock synchronization (MSB/LSB first selectable), 1 channel
 - Timer
 - 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 16-bit capture timer/counter, 32kHz timer/counter
 - I²C bus interface
 - 8-bit pulse measurement counter, 6-stage FIFO
 - PWM output circuit
 - 12 bits, 2 channels
- Interruption
 - 21 factors, 15 vectors, multi-interruption possible
- Standby mode
 - SLEEP/STOP
- Package
 - 80-pin plastic QFP
- Piggyback/evaluation chip
 - CXP84600 80-pin ceramic QFP

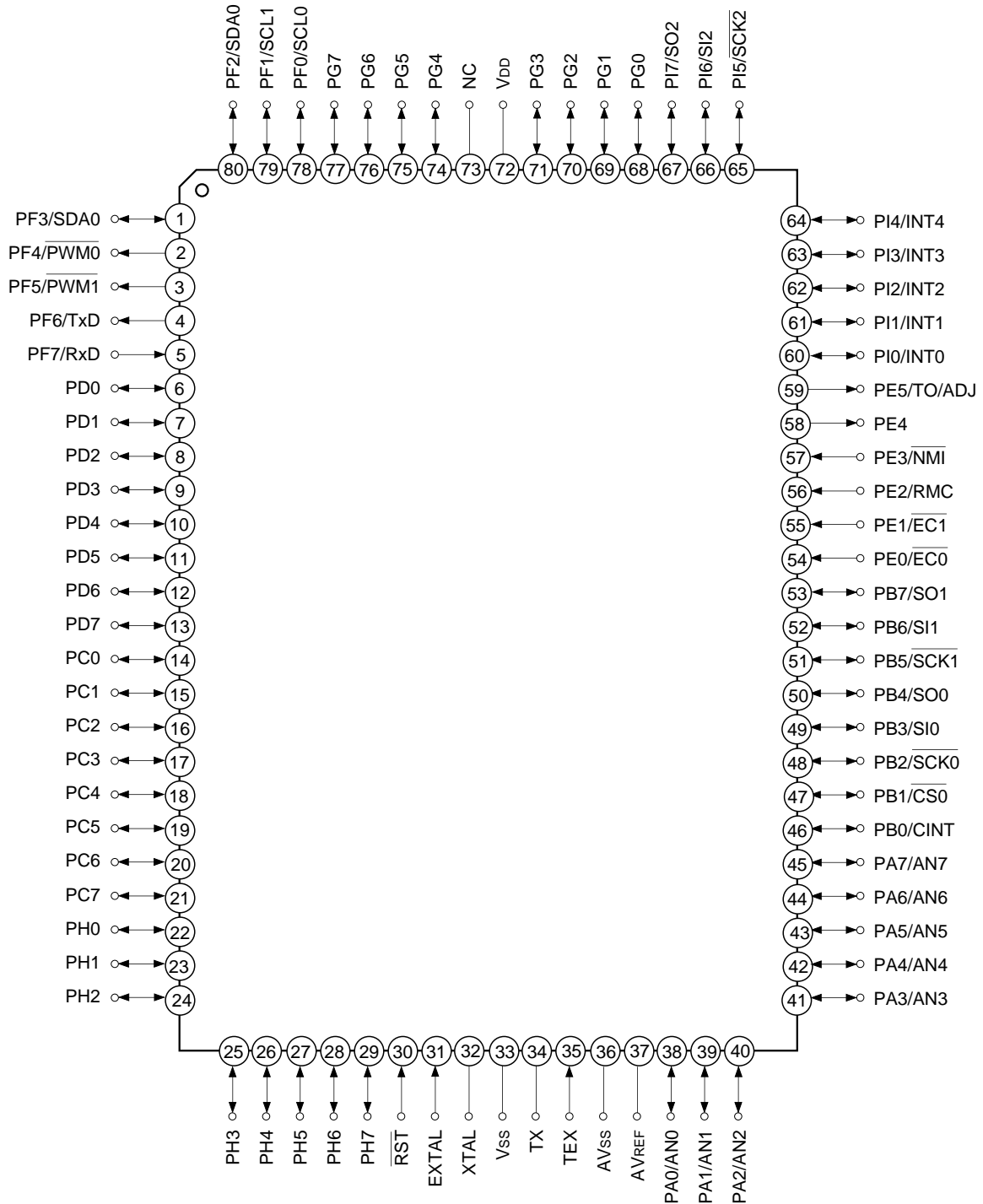
Purchase of Sony's I²C components conveys a licence under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

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Block Diagram

Pin Assignment (Top View)



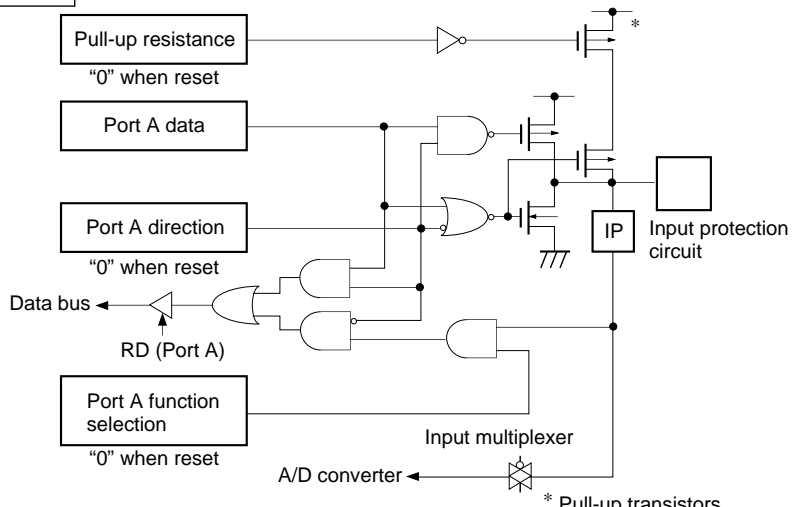
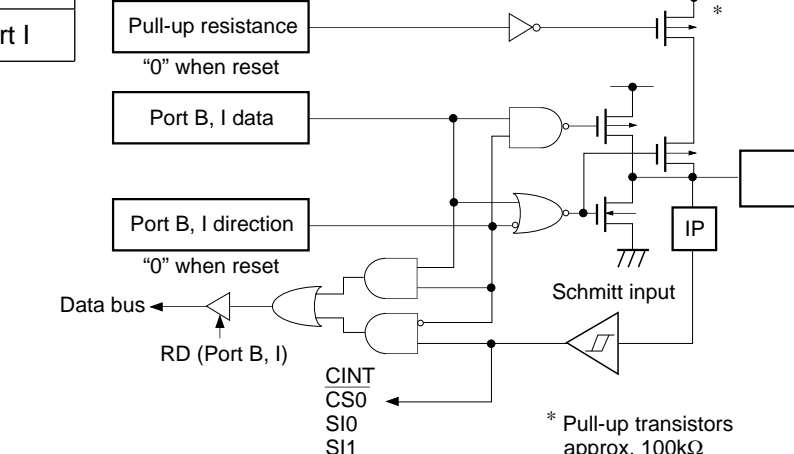
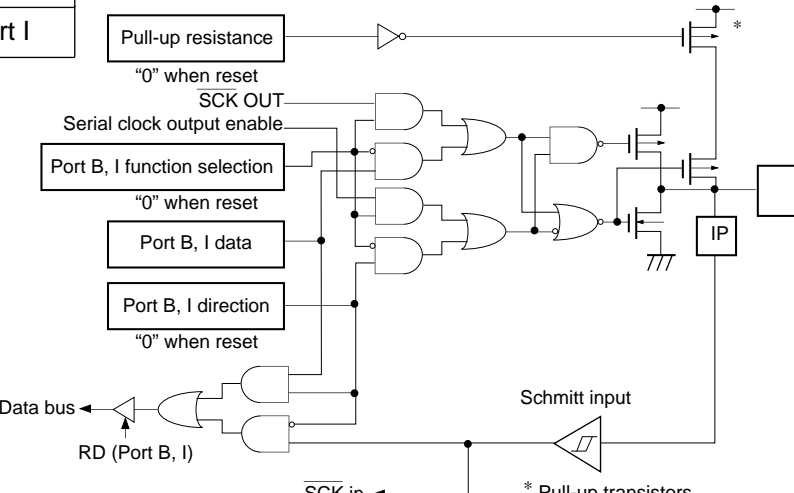
Note) NC (Pin 73) must be connected VDD.

Pin Description

| Pin code | I/O | Functions | |
|--------------------------------|--------------------------|---|---|
| PA0/AN0 to PA7/AN7 | I/O/Analog input | (Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins) | Analog inputs to A/D converter. (8 pins) |
| PB0/CINT | I/O/Input | (Port B) I/O can be set in a unit of single bits for lower 7 bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins) | External capture input to 16-bit timer/counter. |
| PB1/ $\overline{\text{CS}}_0$ | I/O/Input | | Chip select input for serial interface (CH0). |
| PB2/ $\overline{\text{SCK}}_0$ | I/O/I/O | | Serial clock I/O (CH0). |
| PB3/SI0 | I/O/Input | | Serial data input (CH0). |
| PB4/SO0 | I/O/Output | | Serial data output (CH0). |
| PB5/ $\overline{\text{SCK}}_1$ | I/O/I/O | | Serial clock I/O (CH1). |
| PB6/SI1 | I/O/Input | | Serial data input (CH1). |
| PB7/SO1 | I/O/Output | | Serial data output (CH1). |
| PC0 to PC7 | I/O | (Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins) | |
| PD0 to PD7 | I/O | (Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins) | |
| PE0/ $\overline{\text{EC}}_0$ | Input/Input | (Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. (6 pins) | External event inputs for timer/counter. (2 pins) |
| PE1/ $\overline{\text{EC}}_1$ | Input/Input | | Remote control reception circuit input. |
| PE2/RMC | Input/Input | | |
| PE3/ $\overline{\text{NMI}}$ | Input/Input | | |
| PE4 | Output | | |
| PE5/TO/ ADJ | Output/Output/ Output | | Rectangular wave output for 16-bit timer/counter. Output for 32kHz oscillation frequency division. |
| PF0/SCL0 PF1/SCL1 | Output/I/O | (Port F) Lower 7 bits are for output; of which lower 4 bits are large current (12mA) N-ch open drain output. The uppermost bit (PF7) is for input. (8pins) | Transfer clock I/O for I ² C bus interface. (2pins) |
| PF2/SDA0 PF3/SDA1 | Output/I/O | | Transfer data I/O for I ² C bus interface. (2pins) |
| PF4/ $\overline{\text{PWM}}_0$ | Output/Output | | PWM outputs. (2pins) |
| PF5/ $\overline{\text{PWM}}_1$ | Output/Output | | |
| PF6/TxD | Output/Output | | UART transmission data output. |
| PF7/RxD | Input/Input | | UART reception data input. |

| Pin code | I/O | Functions | |
|-------------------------------|------------|---|---|
| PG0 to PG7 | I/O | (Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins) | |
| PH0 to PH7 | I/O | (Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins) | |
| PI0/INT0 to PI4/INT4 | I/O/Input | (Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins) | External interruption request inputs. (5 pins) |
| PI5/ $\overline{\text{SCK2}}$ | I/O/I/O | | Serial clock I/O. (CH2) |
| PI6/SI2 | I/O/Input | | Serial data input. (CH2) |
| PI7/SO2 | I/O/Output | | Serial data output. (CH2) |
| EXTAL | Input | Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL. | |
| XTAL | Output | | |
| TEX | Input | Crystal connectors for 32kHz timer/counter clock oscillation. For usage as event counter, input to TEX, and open TX. | |
| TX | Output | | |
| $\overline{\text{RST}}$ | Input | Low-level active, system reset. | |
| NC | | NC. Under normal operating conditions, connect to V _{DD} . | |
| AV _{REF} | Input | Reference voltage input for A/D converter. | |
| AV _{SS} | | A/D converter GND. | |
| V _{DD} | | Positive power supply. | |
| V _{SS} | | GND. | |

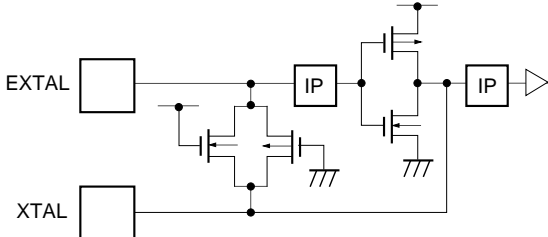
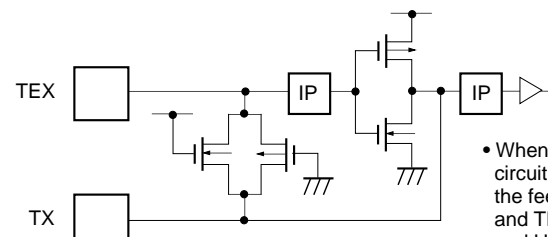
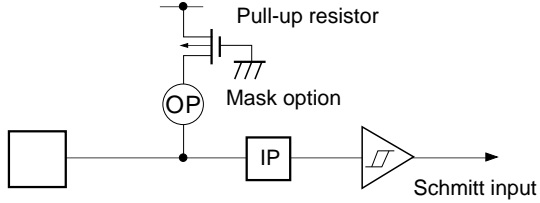
I/O Circuit Format for Pins

| Pin | Circuit format | When reset |
|---|---|-------------|
| <p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p> | <p>Port A</p>  <p>Pull-up resistance "0" when reset</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A function selection "0" when reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>* Pull-up transistors approx. 100kΩ</p> | <p>Hi-Z</p> |
| <p>PB0/CINT PB1/CS0 PB3/SI0 PB6/SI1 PI6/SI2</p> <p>5 pins</p> | <p>Port B Port I</p>  <p>Pull-up resistance "0" when reset</p> <p>Port B, I data</p> <p>Port B, I direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B, I)</p> <p>Schmitt input</p> <p>CINT CS0 SI0 SI1</p> <p>* Pull-up transistors approx. 100kΩ</p> | <p>Hi-Z</p> |
| <p>PB2/SCK0 PB5/SCK1 PI5/SCK2</p> <p>3 pins</p> | <p>Port B Port I</p>  <p>Pull-up resistance "0" when reset</p> <p>SCK OUT Serial clock output enable</p> <p>Port B, I function selection "0" when reset</p> <p>Port B, I data</p> <p>Port B, I direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B, I)</p> <p>Schmitt input</p> <p>SCK in</p> <p>* Pull-up transistors approx. 100kΩ</p> | <p>Hi-Z</p> |

| Pin | Circuit format | When reset |
|---|----------------|------------|
| PB4/SO0 PB7/SO1 PI7/SO2 3 pins | | Hi-Z |
| PC0 to PC7 8 pins | | Hi-Z |
| PE0/EC0 PE1/EC1 PE2/RMC PE3/NMI PF7/RxD 5 pins | | Hi-Z |
| PE4 1 pin | | High level |

| Pin | Circuit format | When reset |
|--|--|--|
| <p>PE5/TO/ADJ</p> <p>1 pin</p> | <p>Port E</p> <p>Internal reset signal</p> <p>Port E data</p> <p>TO</p> <p>ADJ16K*1</p> <p>ADJ2K*1</p> <p>MPX</p> <p>Port E function selection (upper)</p> <p>Port E function selection (lower)</p> <p>"00" when reset</p> <p>TO output enable</p> <p>*1 ADJ signals are frequency dividing output for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.</p> <p>*2 Pull-up transistor approx. 150kΩ</p> | <p>High level (with approx. 150kΩ resistor when reset)</p> |
| <p>PD0 to PD7 PG0 to PG7 PH0 to PH7</p> <p>24 pins</p> | <p>Port D</p> <p>Port G</p> <p>Port H</p> <p>Pull-up resistance</p> <p>"0" when reset</p> <p>Port D, G, H data</p> <p>Port D, G, H direction</p> <p>"0" when reset</p> <p>Data bus</p> <p>RD (Port D, G, H)</p> <p>* Pull-up transistors approx. 100kΩ</p> | <p>Hi-Z</p> |
| <p>PI0/INT0 to PI4/INT4</p> <p>5 pins</p> | <p>Port I</p> <p>Pull-up resistance</p> <p>"0" when reset</p> <p>Port I data</p> <p>Port I direction</p> <p>"0" when reset</p> <p>Data bus</p> <p>RD (Port I)</p> <p>INT0 INT1 INT2 INT3 INT4</p> <p>* Pull-up transistors approx. 100kΩ</p> | <p>Hi-Z</p> |

| Pin | Circuit format | When reset |
|--|---|-------------------|
| <p>PF0/SCL0 PF1/SCL1 PF2/SDA0 PF3/SDA1</p> <p>4 pins</p> | <p>Port F</p> <p>* Large current 12mA</p> | <p>Hi-Z</p> |
| <p>PF4/PWM0 PF5/PWM1</p> <p>2 pins</p> | <p>Port F</p> | <p>High level</p> |
| <p>PF6/TxD</p> <p>1 pin</p> | <p>Port F</p> | <p>High level</p> |
| <p>PH0 to PH7</p> <p>8 pins</p> | <p>Port H</p> | <p>Hi-Z</p> |

| Pin | Circuit format | When reset |
|--|---|--------------------|
| <p>EXTAL XTAL</p> <p>2 pins</p> |  <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop, and XTAL becomes High level. | <p>Oscillation</p> |
| <p>TEX TX</p> <p>2 pins</p> |  <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become Low level and High level respectively. | <p>Oscillation</p> |
| <p>$\overline{\text{RST}}$</p> <p>1 pin</p> |  <p>Pull-up resistor</p> <p>Mask option</p> <p>Schmitt input</p> | <p>Low level</p> |

Absolute Maximum Ratings

(V_{SS} = 0V reference)

| Item | Symbol | Rating | Unit | Remarks |
|---------------------------------|------------------|----------------------------|------|--|
| Supply voltage | V _{DD} | -0.3 to +7.0 | V | |
| | A _{VSS} | -0.3 to +0.3 | V | |
| Input voltage | V _{IN} | -0.3 to +7.0 ^{*1} | V | |
| Output voltage | V _{OUT} | -0.3 to +7.0 ^{*1} | V | |
| High level output current | I _{OH} | -5 | mA | Output (value per pin) |
| High level total output current | ∑I _{OH} | -50 | mA | Total for all output pins |
| Low level output current | I _{OL} | 15 | mA | All pins excluding large current outputs (value per pin) |
| | I _{OLC} | 20 | mA | Large current outputs (value per pin) ^{*2} |
| Low level total output current | ∑I _{OL} | 100 | mA | Total for all output pins |
| Operating temperature | T _{opr} | -20 to +75 | °C | |
| Storage temperature | T _{stg} | -55 to +150 | °C | |
| Allowable power dissipation | P _D | 600 | mW | |

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The large current output is for each pin of Port C (PC), Port F0 (PF0) to Port 3 (PF3).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

| Item | Symbol | Min. | Max. | Unit | Remarks |
|--------------------------|-------------------|-----------------------|-----------------------|------|--|
| Supply voltage | V _{DD} | 4.5 | 5.5 | V | fc = 16MHz or less |
| | | 3.0 | 5.5 | V | fc = 12MHz or less |
| | | 2.7 | 5.5 | V | Guaranteed operation range for 1/16 frequency dividing clock or SLEEP mode |
| | | 2.7 | 5.5 | V | Guaranteed operation range by TEX clock |
| | | 2.5 | 5.5 | V | Guaranteed data hold operation range during STOP |
| High level input voltage | V _{IH} | 0.7V _{DD} | V _{DD} | V | *1, *5 |
| | | 0.8V _{DD} | V _{DD} | V | *1, *6 |
| | V _{IHS} | 0.8V _{DD} | V _{DD} | V | Hysteresis input*2 |
| | V _{IHEX} | V _{DD} - 0.4 | V _{DD} + 0.3 | V | EXTAL pin*3, *5 TEX pin*4, *5 |
| | | V _{DD} - 0.2 | V _{DD} + 0.2 | V | EXTAL pin*3, *6 TEX pin*4, *6 |
| Low level input voltage | V _{IL} | 0 | 0.3V _{DD} | V | *1, *5 |
| | | 0 | 0.2V _{DD} | V | *1, *6 |
| | V _{ILS} | 0 | 0.2V _{DD} | V | Hysteresis input*2 |
| | V _{ILEX} | -0.3 | 0.4 | V | EXTAL pin*3, *5 TEX pin*4, *5 |
| | | -0.3 | 0.2 | V | EXTAL pin*3, *6 TEX pin*4, *6 |
| Operating temperature | T _{opr} | -20 | +75 | °C | |

*1 Normal input port (each pin of PA, PB4, PB7, PC, PF0 to PF4, PG, PH and PI7)

*2 Each pin of $\overline{\text{RST}}$, $\overline{\text{CINT}}$, $\overline{\text{CS0}}$, $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$, SI0, SI1, SI2, $\overline{\text{EC0}}$, $\overline{\text{EC1}}$, RMC, $\overline{\text{NMI}}$, RxD, INT0, INT1, INT2, INT3 and INT4

*3 It is specified only when the external clock is input.

*4 It is specified only when the external event count clock is input.

*5 This case applies to the range of 4.5 to 5.5V supply voltage (V_{DD}).

*6 This case applies to the range of 3.0 to 5.5V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics

Supply voltage (V_{DD}) 4.5 to 5.5V

(T_a = -20 to +75°C, V_{SS} = 0V reference)

| Item | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit |
|--|-------------------|--|--|-------|------|------|------|
| High level output voltage | V _{OH} | PA to PD, PE4, PE5, PF4, PF5, PF6, PG to PI | V _{DD} = 4.5V, I _{OH} = -0.5mA | 4.0 | | | V |
| | | | V _{DD} = 4.5V, I _{OH} = -1.2mA | 3.5 | | | V |
| Low level output voltage | V _{OL} | PA to PD, PE4, PE5, PF4, PF5, PF6, PG to PI | V _{DD} = 4.5V, I _{OL} = 1.8mA | | | 0.4 | V |
| | | | V _{DD} = 4.5V, I _{OL} = 3.6mA | | | 0.6 | V |
| | | PC, PF0 to PF3 | V _{DD} = 4.5V, I _{OL} = 12.0mA | | | 1.5 | V |
| | | PF0 to PF3 (SCL0, SCL1, SDA0, SDA1) | V _{DD} = 4.5V, I _{OL} = 3.0mA | | | 0.4 | V |
| | | PF0 to PF3 (SCL0, SCL1, SDA0, SDA1) | V _{DD} = 4.5V, I _{OL} = 4.0mA | | | 0.6 | V |
| Input current | I _{IHE} | EXTAL | V _{DD} = 5.5V, V _{IH} = 5.5V | 0.5 | | 40 | μA |
| | I _{ILE} | | V _{DD} = 5.5V, V _{IL} = 0.4V | -0.5 | | -40 | μA |
| | I _{IHT} | TEX | V _{DD} = 5.5V, V _{IL} = 5.5V | 0.1 | | 10 | μA |
| | I _{ILT} | | V _{DD} = 5.5V, V _{IL} = 0.4V | -0.1 | | -10 | μA |
| | I _{ILR} | $\overline{\text{RST}}^{*1}$ | V _{DD} = 5.5V, V _{IL} = 0.4V | -1.5 | | -400 | μA |
| | I _{IL} | PA to PD* ² , PG to PI* ² | V _{DD} = 5.5V, V _{IL} = 0.4V | | | -45 | μA |
| | | | V _{DD} = 4.5V, V _{IL} = 4.0V | -2.78 | | | μA |
| I/O leakage current | I _{Iz} | PA to PD* ² , PG to PI* ² , $\overline{\text{RST}}^{*1}$ | V _{DD} = 5.5V V _I = 0, 5.5V | | | ±10 | μA |
| Open drain output leakage current (N-ch Tr off state) | I _{ILOH} | PF0 to PF3 (SCL0, SCL1, SDA0, SDA1) | V _{DD} = 5.5V V _{OH} = 5.5V | | | 10 | μA |
| I ² C bus switch connection impedance (Output Tr off state) | R _{Bs} | SCL0: SCL1 SDA0: SDA1 | V _{DD} = 4.5V V _{SCL0} = V _{SCL1} = 2.25V V _{SDA0} = V _{SDA1} = 2.25V | | | 120 | Ω |

| Item | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit | |
|-------------------|---|--|--|------|------|------|------|--|
| Supply current*3 | I _{DD1} | V _{DD} | 1/2 frequency dividing clock operation | | | | | |
| | | | V _{DD} = 5.5V, 16MHz crystal oscillation (C ₁ = C ₂ = 15pF) | | 31 | 50 | mA | |
| | I _{DD2} | | V _{DD} = 3V, 32kHz crystal oscillation; and termination of 16MHz oscillation (C ₁ = C ₂ = 47pF) | | 40 | 100 | μA | |
| | I _{DDS1} | | SLEEP mode | | | | | |
| | | | V _{DD} = 5.5V, 16MHz crystal oscillation (C ₁ = C ₂ = 15pF) | | 2.5 | 10 | mA | |
| | I _{DDS2} | | V _{DD} = 3V, 32kHz crystal oscillation; and termination of 16MHz oscillation (C ₁ = C ₂ = 47pF) | | 8 | 30 | μA | |
| I _{DDS3} | STOP mode V _{DD} = 5.5V, termination of 16MHz and 32kHz crystal oscillation | | | | 10 | μA | | |
| Input capacity | C _{IN} | PA to PC, PE0 to PE5, PF to PI, EXTAL, <u>TEX</u> , <u>RST</u> | Clock 1MHz 0V for all pins excluding measured pins | | 10 | 20 | pF | |

*1 RST specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*2 PA to PD, and PG to PI specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*3 When all pins are open.

Electrical Characteristics

DC Characteristics

Supply voltage (V_{DD}) 3.0 to 3.6V($T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0\text{V}$ reference)

| Item | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit |
|--|-----------|---|--|---|------|----------|---------------|
| High level output voltage | V_{OH} | PA to PD, PE4, PE5, PF4, PF5, PF6 PC, PF0 to PF3 PF0 to PF3 (SCL0, SCL1, SDA0, SDA1) | $V_{DD} = 3.0\text{V}$, $I_{OH} = -0.15\text{mA}$ | 2.7 | | | V |
| | | | $V_{DD} = 3.0\text{V}$, $I_{OH} = -0.5\text{mA}$ | 2.3 | | | V |
| Low level output voltage | V_{OL} | | $V_{DD} = 3.0\text{V}$, $I_{OL} = 1.2\text{mA}$ | | | 0.3 | V |
| | | | $V_{DD} = 3.0\text{V}$, $I_{OL} = 1.6\text{mA}$ | | | 0.5 | V |
| | | | $V_{DD} = 3.0\text{V}$, $I_{OL} = 5.0\text{mA}$ | | | 1 | V |
| | | | $V_{DD} = 3.0\text{V}$, $I_{OL} = 2.0\text{mA}$ | | | 0.3 | V |
| | | $V_{DD} = 3.0\text{V}$, $I_{OL} = 2.5\text{mA}$ | | | 0.5 | V | |
| Input current | I_{IHE} | EXTAL | $V_{DD} = 3.6\text{V}$, $V_{IH} = 3.6\text{V}$ | 0.3 | | 20 | μA |
| | I_{ILE} | | $V_{DD} = 3.6\text{V}$, $V_{IL} = 0.3\text{V}$ | -0.3 | | -20 | μA |
| | I_{IHT} | TEX | $V_{DD} = 3.6\text{V}$, $V_{IL} = 3.6\text{V}$ | 0.1 | | 10 | μA |
| | I_{ILT} | | $V_{DD} = 3.6\text{V}$, $V_{IL} = 0.4\text{V}$ | -0.1 | | -10 | μA |
| | I_{ILR} | $\overline{\text{RST}}^{*1}$ | $V_{DD} = 3.6\text{V}$, $V_{IL} = 0.3\text{V}$ | -0.9 | | -200 | μA |
| | I_{IL} | PA to PD ^{*2} , PG to PI ^{*2} | | $V_{DD} = 3.0\text{V}$, $V_{IL} = 2.7\text{V}$ | -1.0 | | -20 |
| I/O leakage current | I_{IZ} | PA to PD ^{*2} , PG to PI ^{*2} , $\overline{\text{RST}}^{*1}$ | $V_{DD} = 3.6\text{V}$ $V_I = 0, 3.6\text{V}$ | | | ± 10 | μA |
| Open drain output leakage current (N-ch Tr off state) | I_{LOH} | PF0 to PF3 (SCL0, SCL1, SDA0, SDA1) | $V_{DD} = 3.6\text{V}$ $V_{OH} = 3.6\text{V}$ | | | 10 | μA |
| I ² C bus switch connection impedance (Output Tr off state) | R_{BS} | SCL0: SCL1 SDA0: SDA1 | $V_{DD} = 3.0\text{V}$ $V_{SCL0} = V_{SCL1} = 1.5\text{V}$ $V_{SDA0} = V_{SDA1} = 1.5\text{V}$ | | | 300 | Ω |

| Item | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit |
|------------------|-------------------|---|---|------|------|------|------|
| Supply current*3 | I _{DD1} | V _{DD} | 1/2 frequency dividing clock operation V _{DD} = 3.6V, 12MHz crystal oscillation (C ₁ = C ₂ = 15pF) | | 11 | 25 | mA |
| | I _{DDS1} | | SLEEP mode V _{DD} = 3.6V, 12MHz crystal oscillation (C ₁ = C ₂ = 15pF) | | 0.5 | 2.5 | mA |
| | I _{DDS3} | | STOP mode V _{DD} = 3.6V, termination of 16MHz and 32kHz crystal oscillation | | | 10 | μA |
| Input capacity | C _{IN} | PA to PC, PE0 to PE5, PF to PI, EXTAL, TEX, $\overline{\text{RST}}$ | Clock 1MHz 0V for all pins excluding measured pins | | 10 | 20 | pF |

*1 $\overline{\text{RST}}$ specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*2 PA to PD, and PG to PI specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*3 When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

| Item | Symbol | Pin | Conditions | Min. | Typ. | Max. | Unit |
|--|------------|---------------|---|-------------------|---------|------|------|
| System clock frequency | fc | XTAL EXTAL | Fig. 1, Fig. 2 | VDD = 4.5 to 5.5V | 1 | 16 | MHz |
| | | | | | 1 | 12 | |
| System clock input pulse width | tXL tXH | EXTAL | Fig. 1, Fig. 2 External clock drive | VDD = 4.5 to 5.5V | 28 | | ns |
| | | | | | 37.5 | | |
| System clock input rise time, fall time | tCR tCF | EXTAL | Fig. 1, Fig. 2 External clock drive | | | 200 | ns |
| | | | | | | | |
| Event count input clock pulse width | tEH tEL | EC0 EC1 | Fig. 3 | | 4tsys*1 | | ns |
| | | | | | | | |
| Event count input clock rise time, fall time | tER tEF | EC0 EC1 | Fig. 3 | | | 20 | ms |
| | | | | | | | |
| System clock frequency | fc | TEX TX | VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition) | | 32.768 | | kHz |
| Event count input clock input pulse width | tTL tTH | TEX | Fig. 3 | 10 | | | μs |
| Event count input clock rise time, fall time | tTR tTF | TEX | Fig. 3 | | | 20 | ms |

*1 tsys indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (CLC: 00FEH).

tsys [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (Upper two bits = "11")

Fig. 1. Clock timing

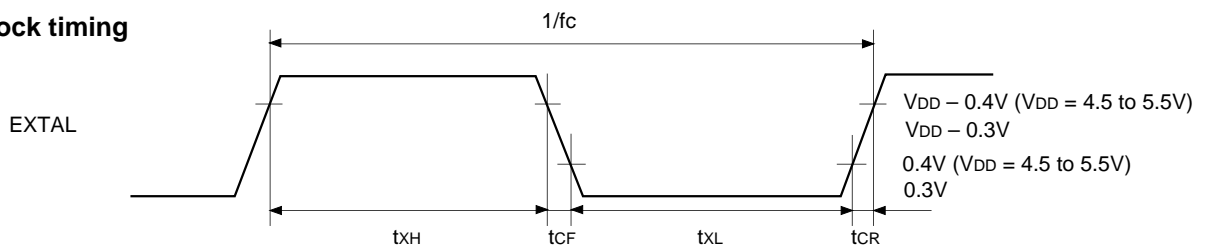


Fig. 2. Clock applied conditions

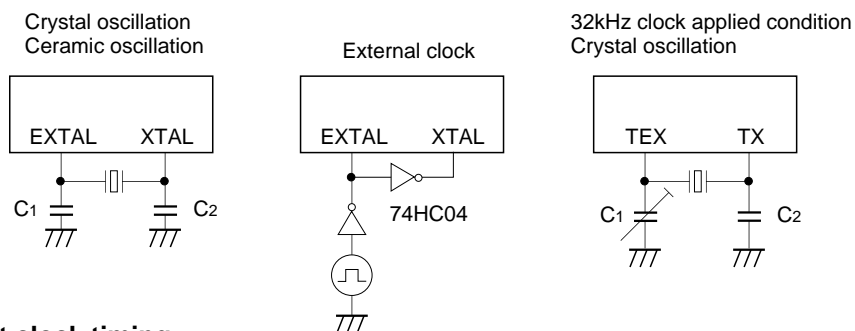
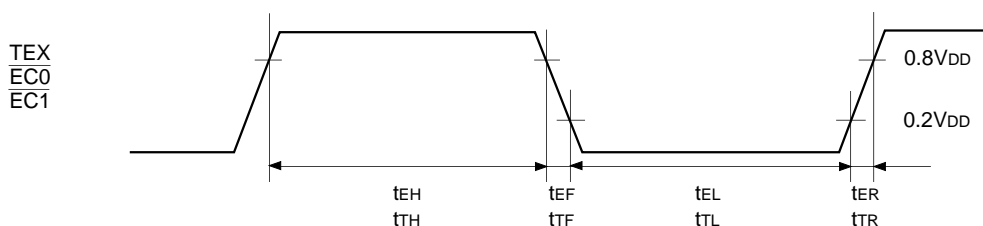


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|---|--|-------------------|---|-------------------------|-------------------------|------|
| $\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time | t _{D_{CSK}} | $\overline{SCK0}$ | Chip select transfer mode (SCK = output mode) | | t _{sys} + 200 | ns |
| $\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time | t _{D_{CSKF}} | $\overline{SCK0}$ | Chip select transfer mode (SCK = output mode) | | t _{sys} + 200 | ns |
| $\overline{CS}\downarrow \rightarrow \overline{SO}$ delay time | t _{D_{CSO}} | SO0 | Chip select transfer mode | | t _{sys} + 200 | ns |
| $\overline{CS}\downarrow \rightarrow \overline{SO}$ floating delay time | t _{D_{CSOF}} | SO0 | Chip select transfer mode | | t _{sys} + 200 | ns |
| \overline{CS} High level width | t _{WH_{CS}} | $\overline{CS0}$ | Chip select transfer mode | t _{sys} + 200 | | ns |
| \overline{SCK} cycle time | t _{K_{CY}} | $\overline{SCK0}$ | Input mode | 2t _{sys} + 200 | | ns |
| | | | Output mode | 16000/fc | | ns |
| \overline{SCK} High and Low level widths | t _{K_H} t _{K_L} | $\overline{SCK0}$ | Input mode | t _{sys} + 100 | | ns |
| | | | Output mode | 8000/fc - 100 | | ns |
| SI input setup time (against $\overline{SCK}\uparrow$) | t _{SIK} | SI0 | \overline{SCK} input mode | -t _{sys} + 100 | | ns |
| | | | \overline{SCK} output mode | 200 | | ns |
| SI input hold time (against $\overline{SCK}\uparrow$) | t _{K_{SI}} | SI0 | \overline{SCK} input mode | 2t _{sys} + 100 | | ns |
| | | | \overline{SCK} output mode | 100 | | ns |
| $\overline{SCK}\downarrow \rightarrow \overline{SO}$ delay time | t _{K_{SO}} | SO0 | \overline{SCK} input mode | | 2t _{sys} + 200 | ns |
| | | | \overline{SCK} output mode | | 100 | ns |

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (upper 2 bits = "00"), 4000/fc (upper 2 bits = "01"), 16000/fc (upper 2 bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO represent $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0, respectively.

Note 3) The load of \overline{SCK} output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, Vss = 0V reference)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|---|------------------------------------|-------------------|---|-------------------------|-------------------------|------|
| $\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time | t _{DCSK} | $\overline{SCK0}$ | Chip select transfer mode (SCK = output mode) | | t _{sys} + 250 | ns |
| $\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time | t _{DCSKF} | $\overline{SCK0}$ | Chip select transfer mode (SCK = output mode) | | t _{sys} + 200 | ns |
| $\overline{CS}\downarrow \rightarrow \overline{SO}$ delay time | t _{DCSO} | SO0 | Chip select transfer mode | | t _{sys} + 250 | ns |
| $\overline{CS}\downarrow \rightarrow \overline{SO}$ floating delay time | t _{DCSOF} | SO0 | Chip select transfer mode | | t _{sys} + 200 | ns |
| \overline{CS} High level width | t _{WHCS} | $\overline{CS0}$ | Chip select transfer mode | t _{sys} + 200 | | ns |
| \overline{SCK} cycle time | t _{KCY} | $\overline{SCK0}$ | Input mode | 2t _{sys} + 200 | | ns |
| | | | Output mode | 16000/fc | | ns |
| \overline{SCK} High and Low level widths | t _{KH} t _{KL} | $\overline{SCK0}$ | Input mode | t _{sys} + 100 | | ns |
| | | | Output mode | 8000/fc - 150 | | ns |
| SI input setup time (against $\overline{SCK}\uparrow$) | t _{SIK} | SI0 | \overline{SCK} input mode | -t _{sys} + 100 | | ns |
| | | | \overline{SCK} output mode | 200 | | ns |
| SI input hold time (against $\overline{SCK}\uparrow$) | t _{KSI} | SI0 | \overline{SCK} input mode | 2t _{sys} + 100 | | ns |
| | | | \overline{SCK} output mode | 100 | | ns |
| $\overline{SCK}\downarrow \rightarrow \overline{SO}$ delay time | t _{KSO} | SO0 | \overline{SCK} input mode | | 2t _{sys} + 250 | ns |
| | | | \overline{SCK} output mode | | 125 | ns |

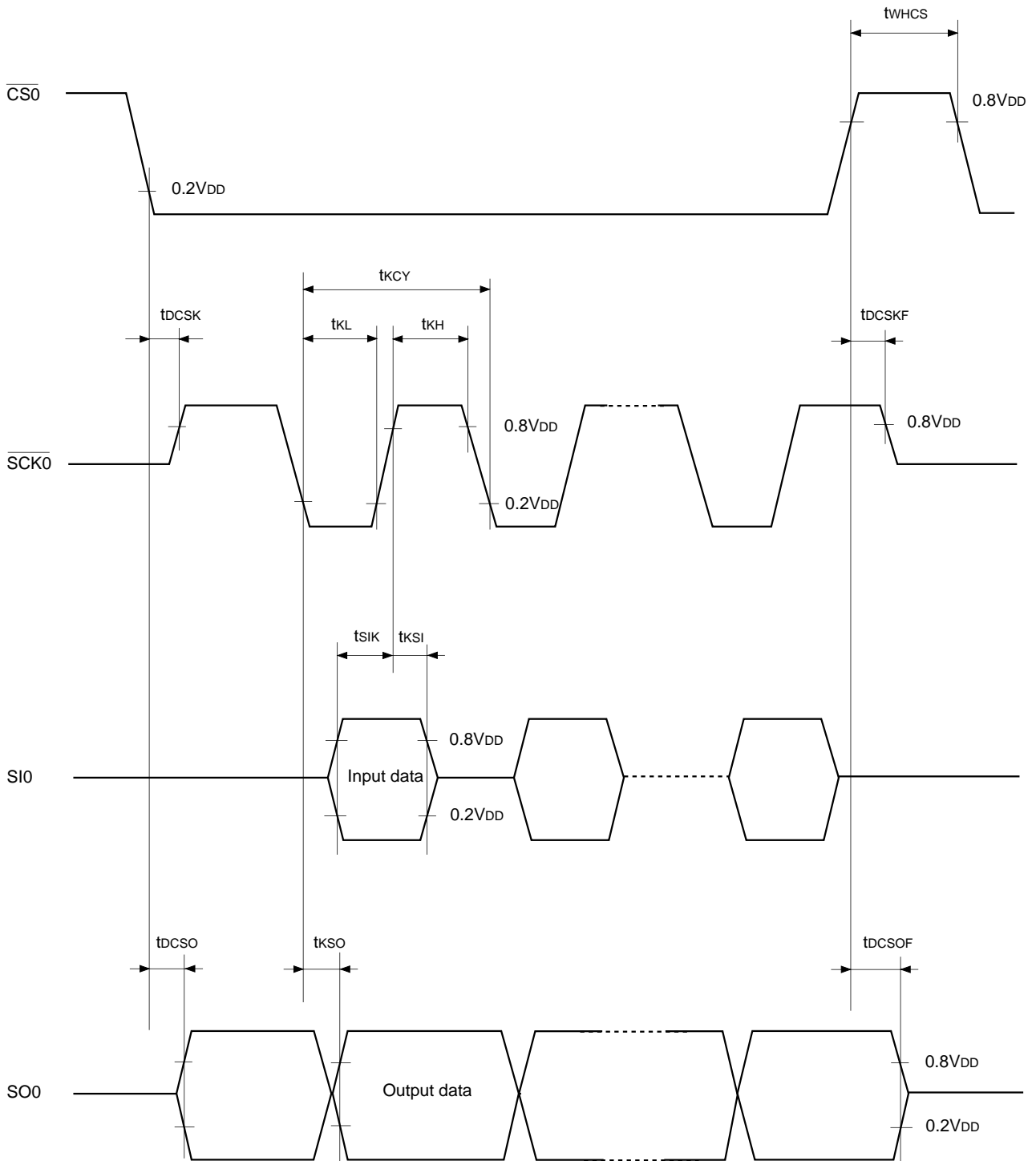
Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (upper 2 bits = "00"), 4000/fc (upper 2 bits = "01"), 16000/fc (upper 2 bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO represent $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0, respectively.

Note 3) The load of \overline{SCK} output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer CH0 timing



Serial transfer (CH1, CH2)

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|--|------------------------------------|--|-------------------------------------|-------------------------|------------------------|------|
| $\overline{\text{SCK}}$ cycle time | t_{KCY} | $\overline{\text{SCK1}}$ $\overline{\text{SCK2}}$ | Input mode | $2t_{\text{sys}} + 200$ | | ns |
| | | | Output mode | $16000/f_c$ | | ns |
| $\overline{\text{SCK}}$ High and Low level widths | t_{KH} t_{KL} | $\overline{\text{SCK1}}$ $\overline{\text{SCK2}}$ | Input mode | $t_{\text{sys}} + 100$ | | ns |
| | | | Output mode | $8000/f_c - 50$ | | ns |
| SI input setup time (against $\overline{\text{SCK}}\uparrow$) | t_{SIK} | SI1 SI2 | $\overline{\text{SCK}}$ input mode | 100 | | ns |
| | | | $\overline{\text{SCK}}$ output mode | 200 | | ns |
| SI input hold time (against $\overline{\text{SCK}}\uparrow$) | t_{KSI} | SI1 SI2 | $\overline{\text{SCK}}$ input mode | $t_{\text{sys}} + 200$ | | ns |
| | | | $\overline{\text{SCK}}$ output mode | 100 | | ns |
| $\text{SCK}\downarrow \rightarrow \text{SO}$ delay time | t_{KSO} | SO1 SO2 | $\overline{\text{SCK}}$ input mode | | $t_{\text{sys}} + 200$ | ns |
| | | | $\overline{\text{SCK}}$ output mode | | 100 | ns |

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2 bits = "00"), 4000/ f_c (Upper 2 bits = "01"), 16000/ f_c (Upper 2 bits = "11")

Note 2) $\overline{\text{SCK}}$, SI and SO represent $\overline{\text{SCK1}}$, SI1, and SO1, respectively for CH1; they represent $\overline{\text{SCK2}}$, SI2 and SO2, respectively for CH2.

Note 3) The load of $\overline{\text{SCK1}}$ and $\overline{\text{SCK2}}$ output modes and SO1 and SO2 output delay times is 50pF+1TTL.

Serial transfer (CH1, CH2)

(Ta = -20 to +75°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V reference)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|--|------------------------------------|--|-------------------------------------|-------------------------|------------------------|------|
| $\overline{\text{SCK}}$ cycle time | t_{KCY} | $\overline{\text{SCK1}}$ $\overline{\text{SCK2}}$ | Input mode | $2t_{\text{sys}} + 200$ | | ns |
| | | | Output mode | $16000/f_c$ | | ns |
| $\overline{\text{SCK}}$ High and Low level widths | t_{KH} t_{KL} | $\overline{\text{SCK1}}$ $\overline{\text{SCK2}}$ | Input mode | $t_{\text{sys}} + 100$ | | ns |
| | | | Output mode | $8000/f_c - 150$ | | ns |
| SI input setup time (against $\overline{\text{SCK}}\uparrow$) | t_{SIK} | SI1 SI2 | $\overline{\text{SCK}}$ input mode | 100 | | ns |
| | | | $\overline{\text{SCK}}$ output mode | 200 | | ns |
| SI input hold time (against $\overline{\text{SCK}}\uparrow$) | t_{KSI} | SI1 SI2 | $\overline{\text{SCK}}$ input mode | $t_{\text{sys}} + 200$ | | ns |
| | | | $\overline{\text{SCK}}$ output mode | 100 | | ns |
| $\text{SCK}\downarrow \rightarrow \text{SO}$ delay time | t_{KSO} | SO1 SO2 | $\overline{\text{SCK}}$ input mode | | $t_{\text{sys}} + 250$ | ns |
| | | | $\overline{\text{SCK}}$ output mode | | 125 | ns |

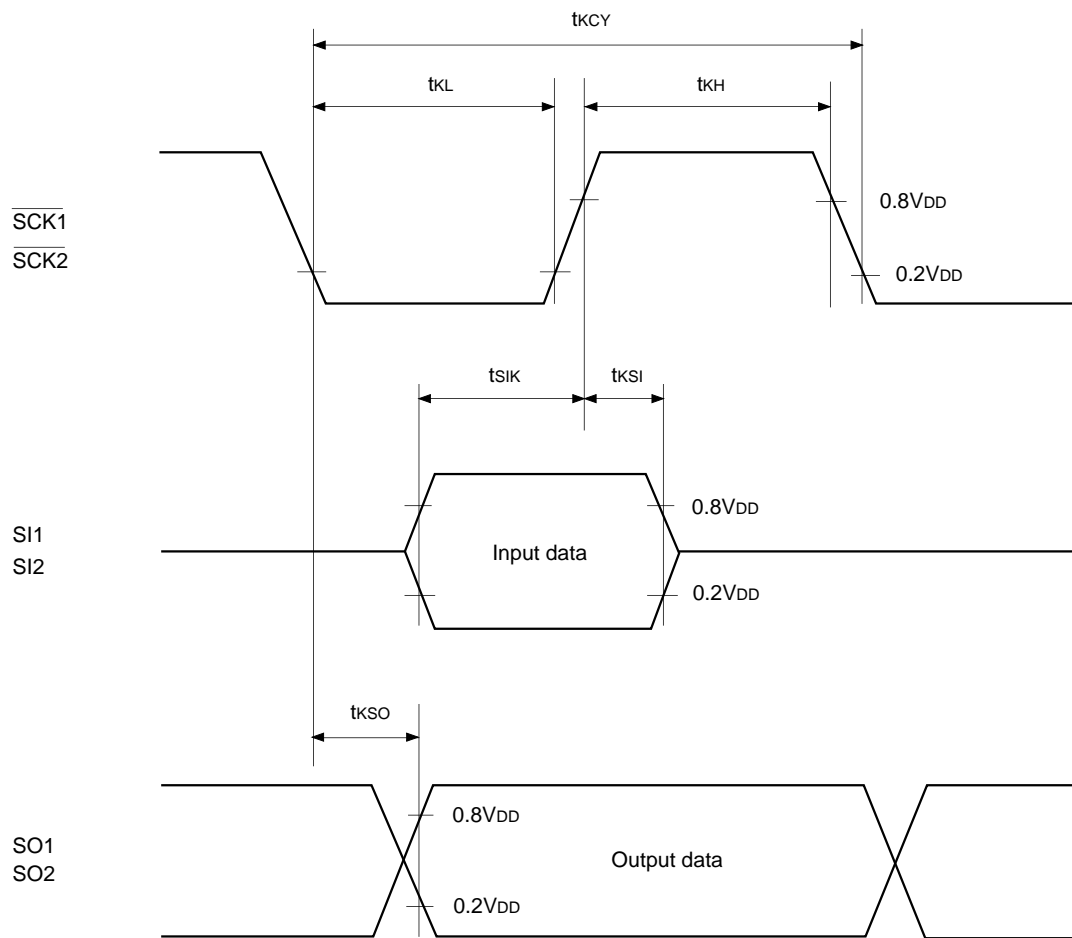
Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2 bits = "00"), 4000/ f_c (Upper 2 bits = "01"), 16000/ f_c (Upper 2 bits = "11")

Note 2) $\overline{\text{SCK}}$, SI and SO represent $\overline{\text{SCK1}}$, SI1, and SO1, respectively for CH1; they represent $\overline{\text{SCK2}}$, SI2 and SO2, respectively for CH2.

Note 3) The load of $\overline{\text{SCK1}}$ and $\overline{\text{SCK2}}$ output modes and SO1 and SO2 output delay times is 50pF.

Fig. 5. Serial transfer CH1 and CH2 timing

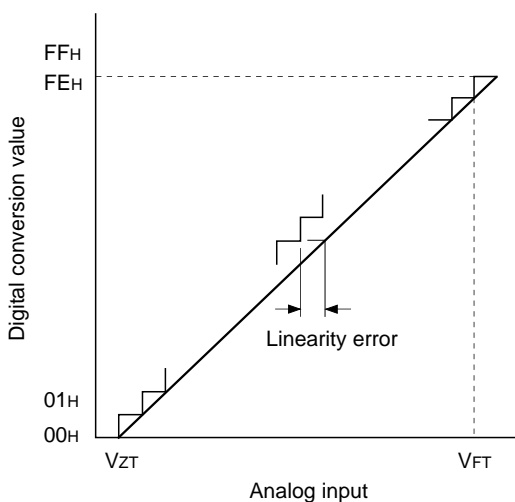


(3) A/D converter characteristics

(Ta = -20 to +75°C, VDD = 3.0 to 5.5V, AVREF = 2.7 to VDD, VSS = AVSS = 0V reference)

| Item | Symbol | Pin | Condition | Min. | Typ. | Max. | Unit | |
|-------------------------------|--------|------------|--|------------|------|-------|------|----|
| Resolution | | | | | | 8 | Bits | |
| Linearity error | | | Ta = 25°C VDD = AVREF = 5.0V VSS = AVSS = 0V | | | ±3 | LSB | |
| Zero transition voltage | VZT*1 | | | -50 | 10 | 70 | mV | |
| Full-scale transition voltage | VFT*2 | | | 4910 | 4970 | 5030 | mV | |
| Linearity error | | | Ta = 25°C VDD = AVREF = 3.3V VSS = AVSS = 0V | | | ±5 | LSB | |
| Zero transition voltage | VZT*1 | | | -10 | 6.5 | 70 | mV | |
| Full-scale transition voltage | VFT*2 | | | 3215 | 3280 | 3345 | mV | |
| Conversion time | tCONV | | | 160/fADC*3 | | | µs | |
| Sampling time | tsAMP | | | 12/fADC*3 | | | µs | |
| Reference input voltage | VREF | AVREF | VDD = 4.5 to 5.5V | VDD - 0.5 | | VDD | V | |
| | | | VDD = 3.0 to 3.6V | VDD - 0.3 | | VDD | V | |
| Analog input voltage | VIAN | AN0 to AN7 | | 0 | | AVREF | V | |
| AVREF current | IREF | AVREF | Operation mode | VDD = 5.5V | | 0.6 | 1.0 | mA |
| | | | | VDD = 3.6V | | 0.4 | 0.7 | mA |
| | IREFS | | SLEEP mode STOP mode 32kHz operation mode | | | | 10 | µA |

Fig.6. Definition of A/D converter terms



*1 VZT: Value at which the digital conversion value changes from 00H to 01H and vice versa.

*2 VFT: Value at which the digital conversion value changes from FEH to FFH and vice versa.

*3 fADC indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9H) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: 00FEH).

| CKS PCK1, PCK0 | 0(φ/2 selection) | 1(φ selection) |
|-------------------|------------------|----------------|
| | 00 (φ = fEX/2) | fADC = fc/2 |
| 01 (φ = fEX/4) | fADC = fc/4 | fADC = fc/2 |
| 11 (φ = fEX/16) | fADC = fc/16 | fADC = fc/8 |

(4) Interruption, reset input ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|--|----------------------|---|-----------|----------|------|---------------|
| External interruption High, Low level width | t_{IH} t_{IL} | INT0 INT1 INT2 INT3 INT4 $\overline{\text{NMI}}$ | | 1 | | μs |
| Reset input Low level width | t_{RSL} | $\overline{\text{RST}}$ | | $32/f_c$ | | μs |

Fig. 7. Interruption input timing

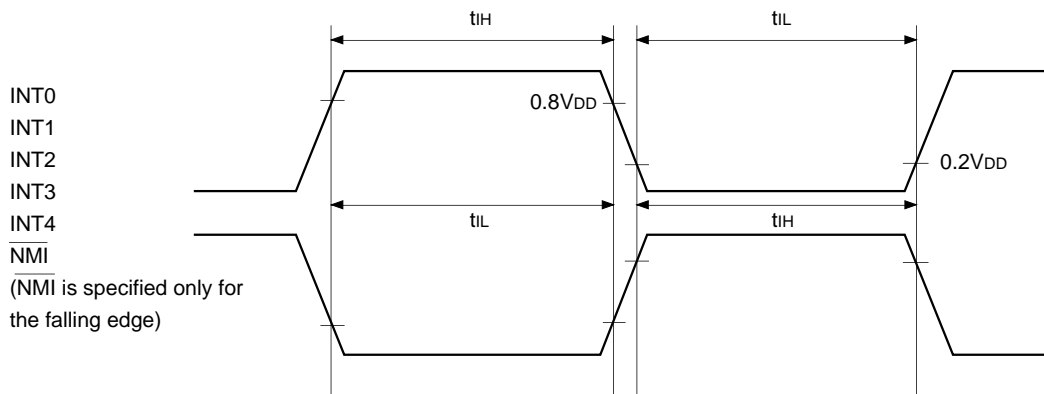
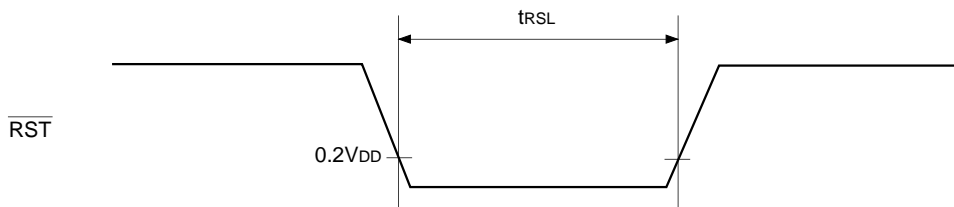


Fig. 8. $\overline{\text{RST}}$ input timing



(5) I²C bus timing

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|--|----------------------|----------|-----------|------|------|------|
| SCL clock frequency | f _{SCL} | SCL | | 0 | 100 | kHz |
| Bus-free time before starting transfer | t _{BUF} | SDA, SCL | | 4.7 | | μs |
| Hold time for starting transfer | t _{HD; STA} | SDA, SCL | | 4.0 | | μs |
| Clock Low level width | t _{LOW} | SCL | | 4.7 | | μs |
| Clock High level width | t _{HIGH} | SCL | | 4.0 | | μs |
| Setup time for repetitive transfers | t _{SU; STA} | SDA, SCL | | 4.7 | | μs |
| Data hold time | t _{HD; DAT} | SDA, SCL | | 0*1 | | μs |
| Data setup time | t _{SU; DAT} | SDA, SCL | | 250 | | ns |
| SDA, SCL rise time | t _R | SDA, SCL | | | 1 | μs |
| SDA, SCL fall time | t _F | SDA, SCL | | | 300 | ns |
| Setup time for transfer completion | t _{SU; STO} | SDA, SCL | | 4.7 | | μs |

*1 The data hold time must exceed 300ns because the SCL rise time (300ns max.) is not taken into consideration.

Fig. 9. I²C bus transfer timing

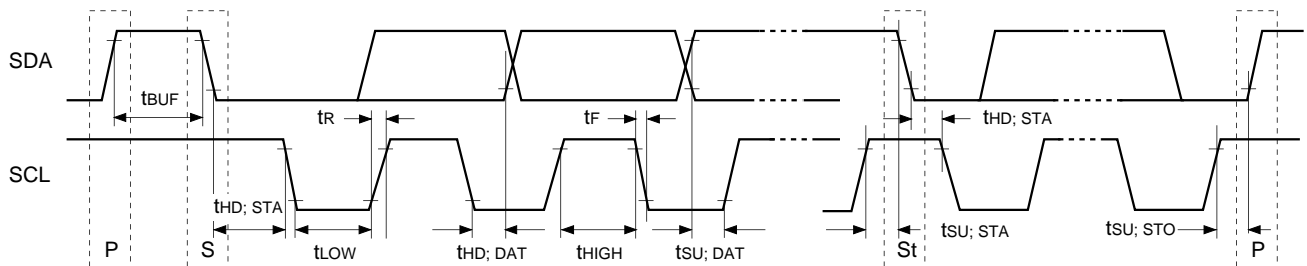
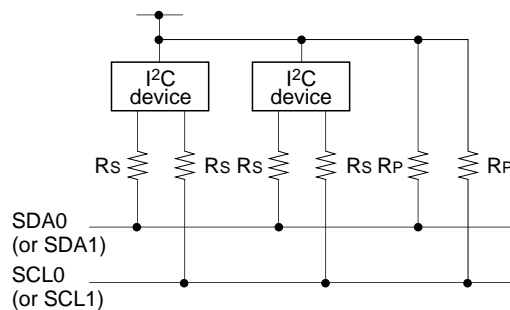


Fig. 10. Recommended circuit example for I²C device



- Pull-up resistors (R_P) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- Serial resistance (R_s = 300Ω or less) of SDA0 (or SDA1) and SCL0 (or SCL1) reduces spike noise caused by CRT flash-over.

Appendix

Fig. 11. SPC700 Series recommended oscillation circuit

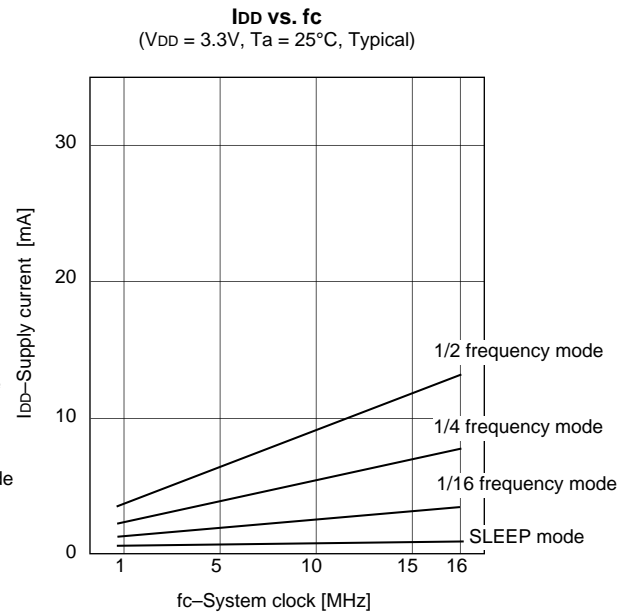
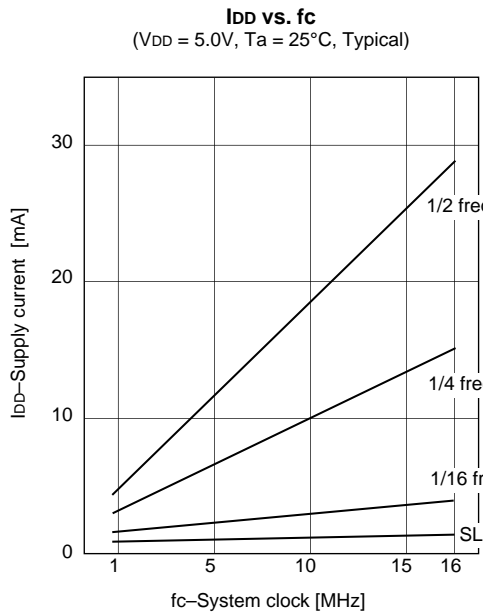
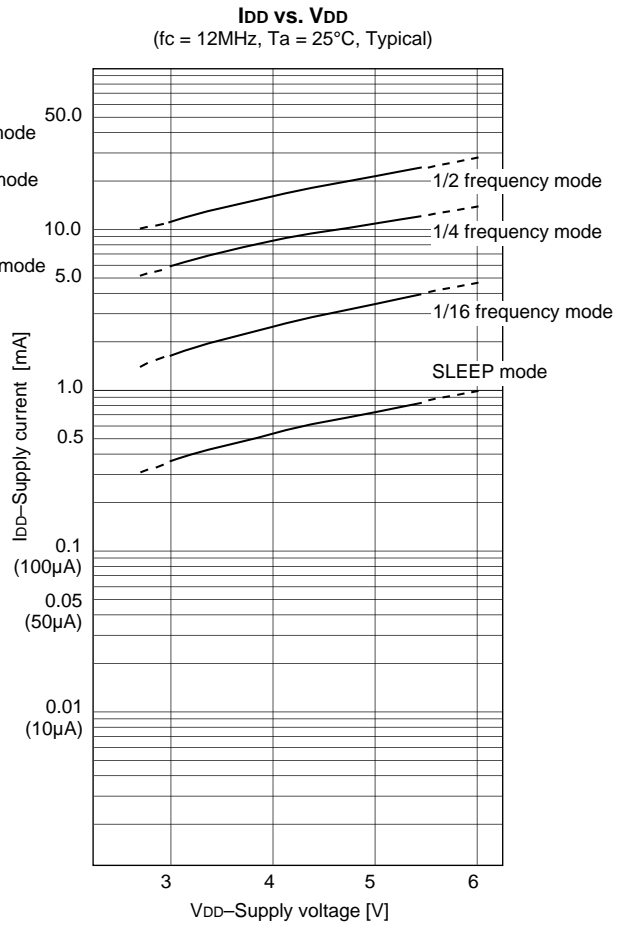
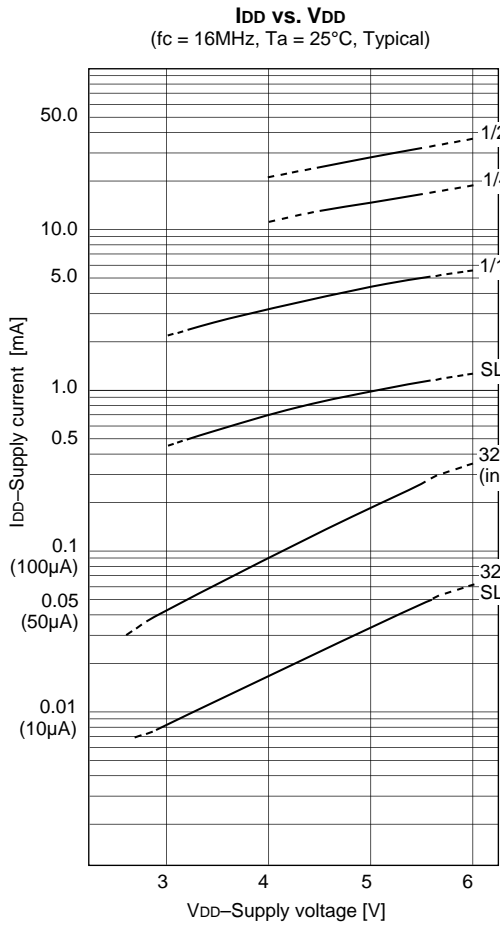


| Manufacturer | Model | fc (MHz) | C1 (pF) | C2 (pF) | Rd (Ω) | Circuit example |
|------------------------|--------------|-----------|---------|---------|-----------------|-----------------|
| RIVER ELETEC CO., LTD. | HC-49/U03 | 8.00 | 10 | 10 | 0 | (i) |
| | | 10.00 | 5 | 5 | | |
| | | 12.00 | | | | |
| | | 16.00 | | | | |
| KINSEKI LTD. | HC-49/U (-S) | 8.00 | 16 (12) | 16 (12) | 0 | (i) |
| | | 10.00 | 16 (12) | 16 (12) | 0 | |
| | | 12.00 | 12 | 12 | 0 | |
| | | 16.00 | 12 | 12 | 0 | |
| | P3 | 32.768kHz | 30 | 18 | 470k | (ii) |

Mask option table

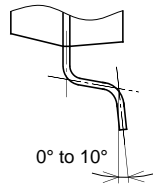
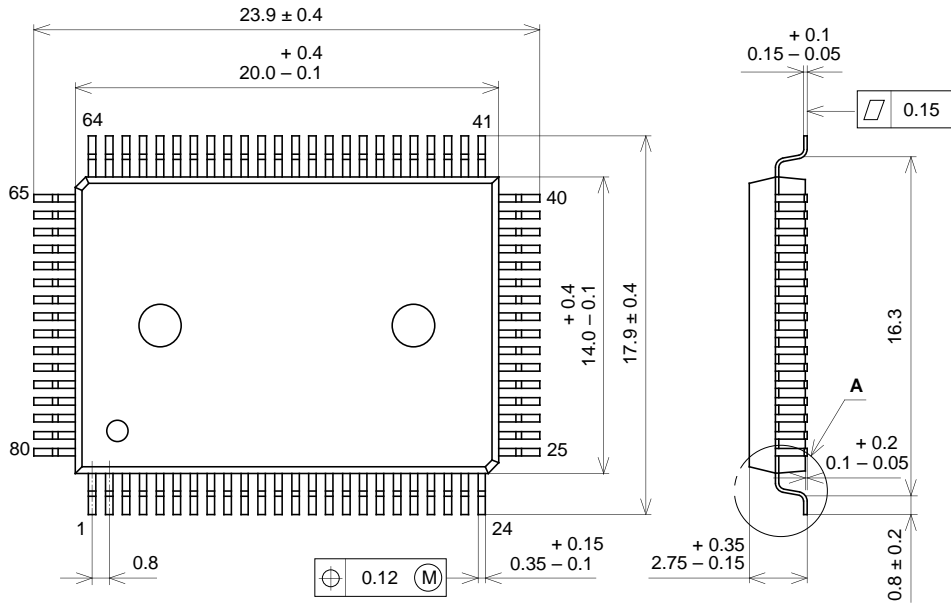
| Item | Content | |
|------|----------------------------|--------------|
| | Reset pin pull-up resistor | Non-existent |

Characteristics Curve



Package Outline Unit: mm

80PIN QFP (PLASTIC)



DETAIL A

| | |
|------------|------------------|
| SONY CODE | QFP-80P-L01 |
| EIAJ CODE | *QFP080-P-1420-A |
| JEDEC CODE | _____ |

PACKAGE STRUCTURE

| | |
|------------------|-------------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | COPPER / 42 ALLOY |
| PACKAGE WEIGHT | 1.6g |